What is claimed is:

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1. A process of designing an integrated circuit comprising:

determining a specification for the integrated circuit;

mapping functions to the specification, the functions being comprised of groups; and

determining the placement of the functions in a layout.

- 2. The process of designing an integrated circuit of claim 1 wherein the functions are of a plurality of predefined sizes and shapes.
- 3. The process of designing an integrated circuit of claim 2 wherein the groups are of a plurality of predefined sizes and shapes.
- 4. The process of designing an integrated circuit of claim 3 wherein the groups have predefined interconnection points.
- 5. The process of designing an integrated circuit of claim 4 wherein the groups each provide one of a plurality of logic functions.
- 6. The process of designing an integrated circuit of claim 5 wherein multiple groups, each of a different size and shape, provide the same logic function.
- 7. The process of designing an integrated circuit of claim 6 further comprising mapping groups to the specification and determining placement of the groups in the layout.
- 8. The process of designing an integrated circuit of claim 7 wherein the groups define a physical representation of a logic circuit.
- 1 9. The process of designing an integrated circuit of claim 8 wherein 2 the groups are defined by GDSIII files.
- 1 10. The process of designing an integrated circuit of claim 9 wherein 2 the groups are comprised of on the order of 1000 gates.
 - 11. A method of determining a definition of a physical representation of at least a portion of an integrated circuit, the integrated circuit performing logic



3	operations, arithmetic operations, control operations, and memory operations, the			
4	integrated circuit being comprised of a plurality of groups the groups being largely			
5	comprised of between 300 and 5000 gates, the groups being present in a library of groups			
6	with each group being predefined in terms of logical and physical layouts, the physical			
7	layouts having predefined boundaries with predefined interconnection points along the			
8	physical boundaries, and at least some of the groups being amalgamated into functions,			
9	the functions being present in a library of function, the method comprising:			
10	selecting an item, the item being a group or a function, for			
11	placement on a layout;			
12	placing the item on the layout;			
13	selecting a further item for placement on the layout;			
14	plaging the further item on the layout; and			
15	defining interconnections between the item and the further item.			
1	12. The method of claim 11 wherein the layout comprises a plurality	ΩÍ		
2	layers.	U		
2	layers.			
1	13. The method of claim 12 wherein the plurality of layers are			
2	separated by metalization having vias			
1	14. An integrated circuit comprised of a plurality of regularly placed			
2	circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit	u11		
3	groups having predefined connection points, at least some of the circuit groups being			
4	amalgamated into sets of groups.			
1	15. The integrated circuit of claim 14 further comprising trailers			
2	attached to groups.			
1	16. The integrated circuit of claim 15 wherein the trailers provide			
2	physical translation of interface signals associated with the predefined connection point	s.		
1	17. The integrated circuit of claim 15 wherein the trailers provide for	• ·		
2	buffering of interface signals associated with the predefined connection points.			
1	18. The integrated circuit of claim 15 wherein the trailers provide for			
2	staging of interface signals associated with the predefined connections points.			
_	submits of interface signals associated with the predefined confidentials points.			

1	19. The integrated circuit of claim 14 wherein the integrated circuit has		
2	a number of metal layers, with the plurality of circuit groups on a first plurality of metal		
3	layers and clock and power signals on metal layers other than the first plurality of metal		
4	layers.		
1	20. The integrated circuit of claim 19 wherein the clock and power		
	signals are on the same metal layer.		
2	signals are on the same metal layer.		
1	21. The integrated circuit of claim 20 wherein global routing signals		
2	are on a metal layer other than the first plurality of metal layers or the metal layer of the		
3	clock and power signals.		
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1	22. The integrated circuit of claim 21 wherein the global routing		
2	signals are on a plurality of metal layers.		
1	23. The integrated circuit of claim 19 wherein the groups comprise		
2	data path groups and memory groups.		
1	24. The integrated circuit of claim 23 wherein the groups further		
2	comprise control groups.		
1	25. The integrated circuit of claim 24 wherein the groups further		
2	comprise I/O groups.		
1	26. The integrated circuit of claim 25 wherein the groups further		
2	comprise analog groups.		
1	27. A process of designing an electronic logic system, the process		
	•		
) 3	comprising:		
_	mapping groups to a functional description, the groups being		
4	comprised of up to 5000 gates, the groups being partitioned into data path groups, contro		
5	groups, memory groups, I/O groups, and analog groups;		
6	testing functional models of the mapped groups to verify the		
7	functional correctness of the mapping of groups to the functional description;		

	8		performing timing, area, and power estimation using detailed
	9	physical models of the	ie mapped groups; and
	10		importing implementation files into the design.
	1	28.	The process of designing an electronic logic system of claim 27
	2	wherein the groups a	re predefined in terms of behavior, timing, power, and physical
	3	layout.	
	1	29.	The process of designing an electronic logic system of claim 28
	2	wherein different set	s of groups implement different functions.
	1	30.	The process of designing an electronic logic system of claim 29
	2	wherein groups with	in a set of groups implementing a function implement different
	3	behavior.	
: :	1	31.	The process of designing an electronic logic system of claim 29
	2	wherein groups with	in a set of groups implementing a function have different physical
	3	layouts.	
	1	32.	The process of designing an electronic logic system of claim 29
	2	wherein groups with	in a set of groups implementing a function have different power
	3	usage.	